

WHITEPAPER: Designed, Verified and Embedded - Winning with SoC Designs in FPGAs

Category: Methodology

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Applies To: see the bottom of this document

With the start of each new SoC project, engineering managers are faced with the challenge of developing the product on schedule and getting it out ahead of the competition. A key element that determines the speed of product development is the set of tools available to developers. Good tools can speed up manual and time-consuming operations for both development and verification and at the same time enhance product quality and other parameters. Another important factor is the methodology used for design development and testing. One of the main challenges on any project is harmonious and effective cooperation between the hardware designers and software developers. The situation can become strained if software developers using ISS and software models need to wait for operational hardware, wasting time and money. With the right tools a team manager can help the team to their increase productivity, minimize idle time, and get SoC projects out on schedule and ahead of the competition.

Bridging the Gap between Hardware and Software Engineers

Aldec is developing a solution to help engineering managers overcome the current SoC project challenges for both their hardware and software engineers. Leveraging Actel Corporation's flash-based M7 ProASIC3 FPGA and the company's new CoreMP7, a soft ARM7-based processor core, this solution supports all stages of product development, including instantaneous software verification on the real hardware. The product also offers strong concurrent hardware and software debugging capabilities.

The Aldec solution includes:

- 1) Link to Actel CoreConsole IP Deployment Platform (IDP)
- 2) Link to Actel Libero integrated design environment (IDE)
- 3) Aldec HDL simulator
- 4) Aldec HES acceleration board based on Actel M7 ProASIC3 devices
- 5) Aldec DVM application for setup management
- 6) ARM RealView debugger interface for Actel CoreMP7 soft ARM7 processor*.

* Supports ARM AXD Real View Debugger.

Development Flow

Let's assume that we want to create an ARM-based voice recognition device according to the system diagram shown in Figure 1. The recognition system can be divided into two domains: software and hardware. The software section, managed by the ARM processor, performs character extraction, data framing and system management. The hardware section performs the pattern detection and processing, using the pattern database memory. The results of the hardware calculations are transferred to the software domain controlled by the ARM processor.

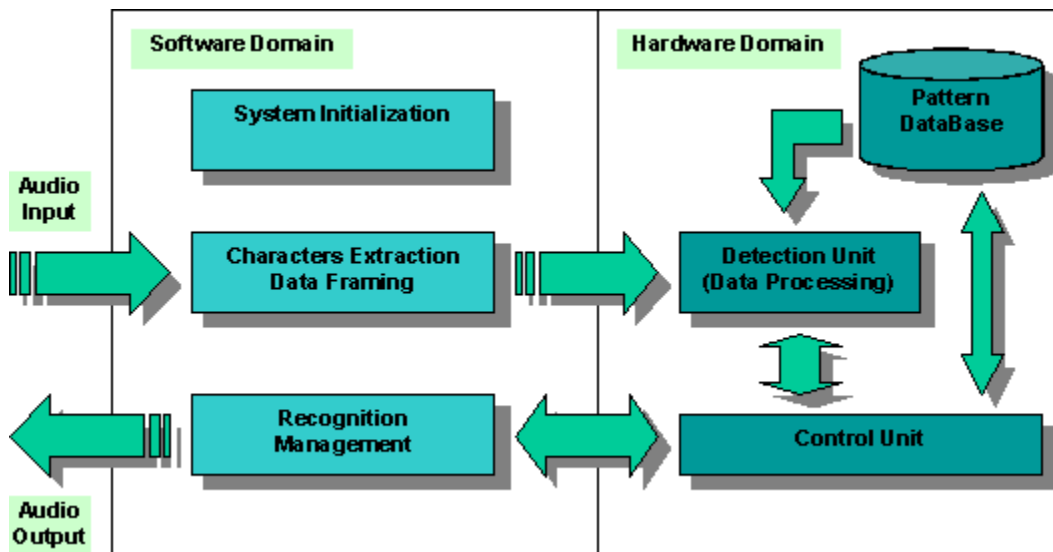


Fig. 1 Voice Recognition System – General Diagram.

After defining the hardware and software sections, we can begin the SoC development stage. The Actel CoreConsole IDP is the starting point for hardware designers. CoreConsole is a system-level configuration utility that allows the developer to stitch together intellectual property (IP) blocks using the AHB bus fabric. It generates a system testbench, controlled by a script-driven, bus functional model (BFM) of the CoreMP7 processor. The BFM allows the developer to model low-level bus transactions, allowing verification of IP block connectivity and the system memory map, presented to the CoreMP7 by the rest of the hardware. The CoreConsole IDP creates a system project with a SPIRIT-compliant description in XML for other tools to import the CoreMP7-based system. This project can be imported into Aldec's DVM setup manager or can be directly imported into the Actel Libero IDE for simulation, synthesis, layout and bitstream generation for the FPGA.

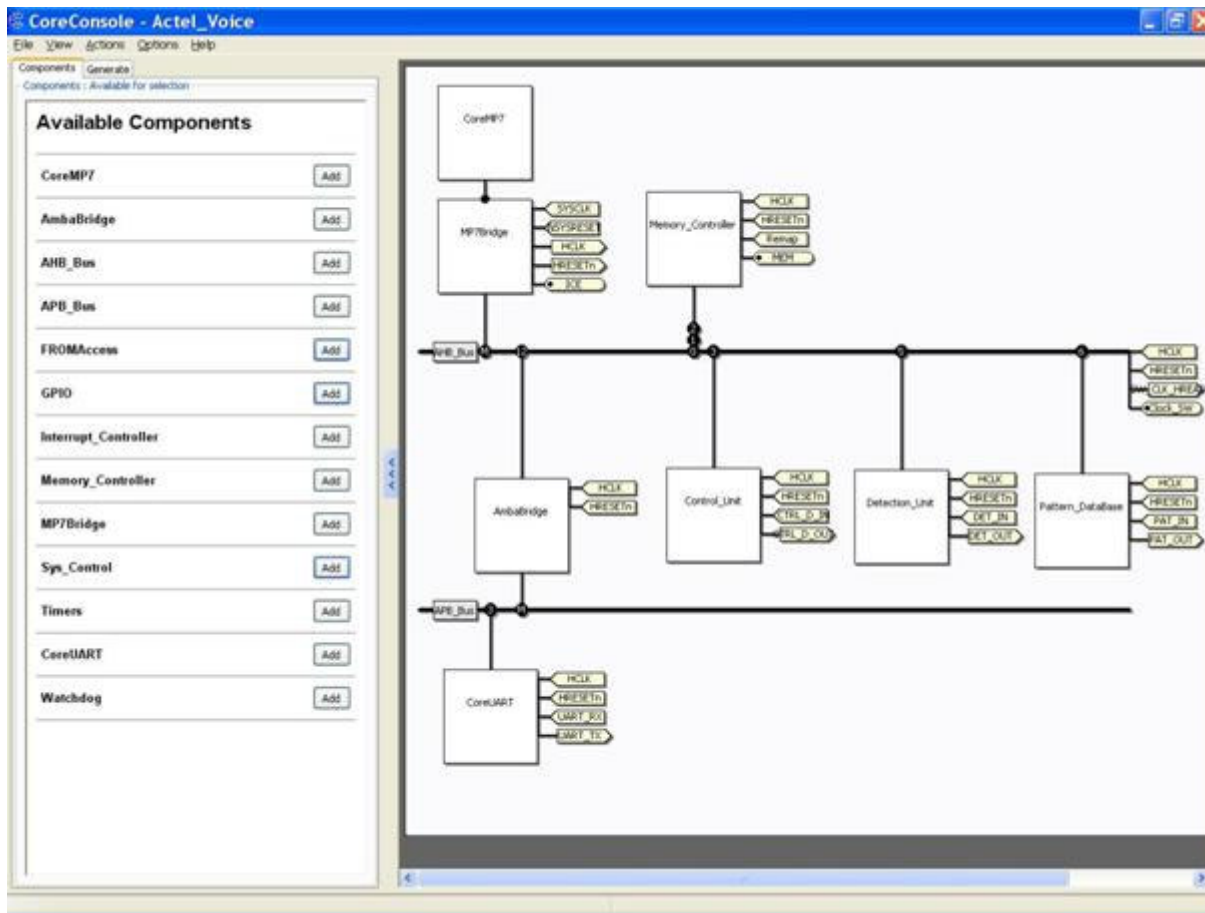


Fig. 2 Voice Recognition System structure in Actel's CoreConsole IDP.

With the hardware engineers working on system configuration and IP core integration, the software developers, using the ARM RealView environment, can concurrently develop the ARM software subroutines and compile the binaries for the hardware verification platform (Actel CoreMP7/M7 ProASIC3).

When the hardware part of the system is ready, CoreConsole generates the hardware description of the design in either Verilog or VHDL for logic synthesis along with the memory map files that can be used in software development. The generated design consists of the encrypted CoreMP7 as a blackbox that has already been pre-placed and routed on the FPGA, along with the configured peripherals and AHB bus fabric in RTL. Logic designers can perform their normal design flow through synthesis, simulation and physical design.

Co-Verification Flow

The next step is importing of the CoreConsole design to Aldec's DVM setup manager. Aldec's patented HES (Hardware Embedded Simulation) environment allows integration of software IP cores with hardware design blocks into one fully operational environment. HES is driven by DVM which allows mapping of the hardware blocks into the hardware-software environment. The peripherals that have been verified in the simulator can be downloaded to the HES board to produce faster simulation and verification in hardware (Actel M7 ProASIC3 device). Hardware modules, which are still under development, can stay in the simulator for further editing and software simulations. Once verified, they can also be assigned to the HES board. Debugging signals can be defined in the DVM application. After the setup, all auxiliary files required for co-verification are automatically generated. With the Actel Libero IDE integrated with DVM, the bit file for the device is also created.

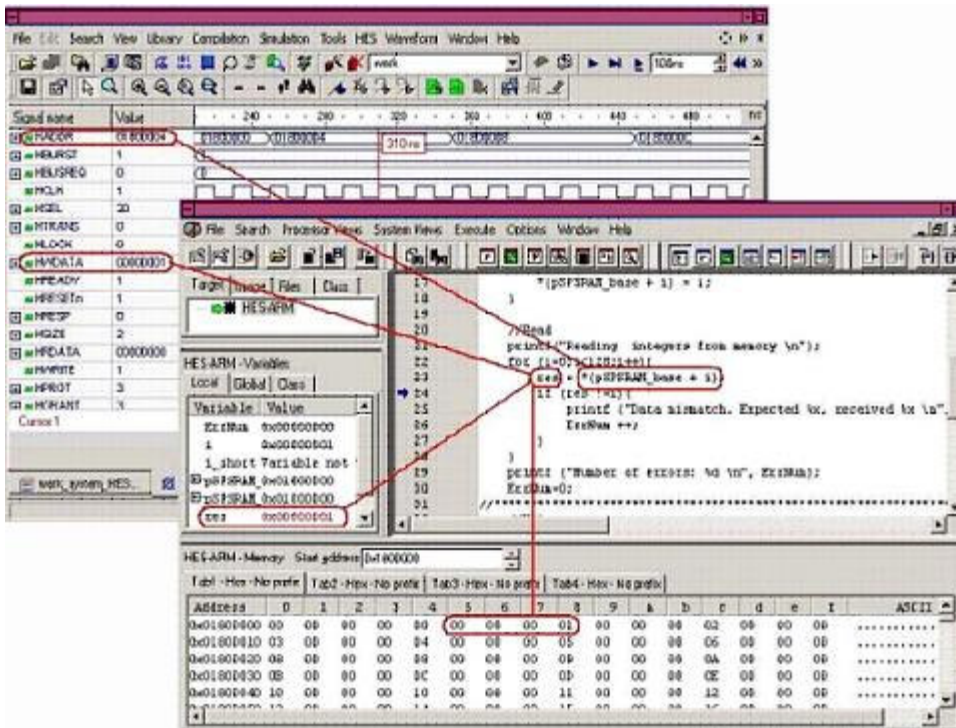


Fig. 4 Parallel debug of the processor (ARM AXD) and AHB peripherals (Aldec Active-HDL).

The above-described hardware-software environment provides for instantaneous and concurrent co-verification of hardware and software design sections, shortening the development cycle of the project. Software developers no longer need to wait for the hardware environment, and hardware designers can work with the latest version of the processor firmware. By providing integrated simulation and debugging of the peripherals and the processor, the Aldec ARM7 co-verification solution helps engineering managers overcome SoC design challenges enabling them to increase productivity, minimize idle time, and get their projects out on schedule and ahead of the competition.

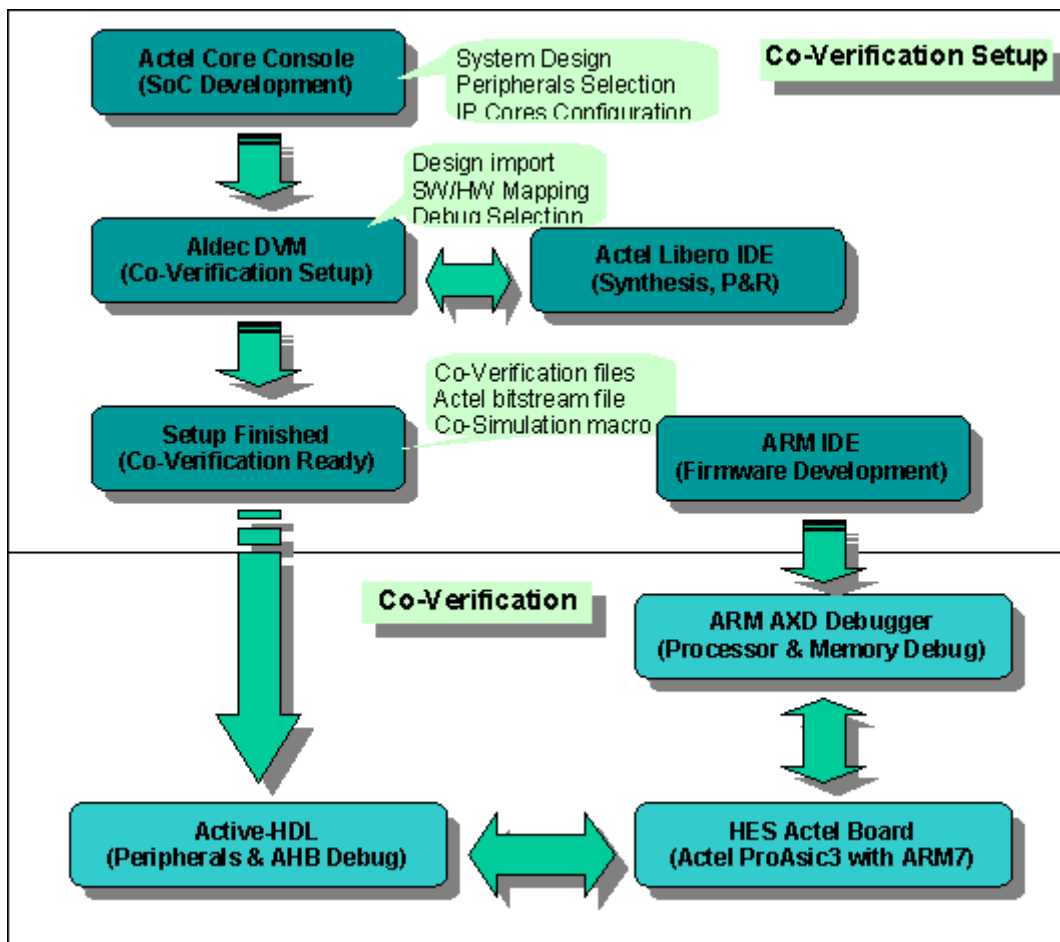


Fig. 5 Aldec-Actel Co-Verification Flow for SoC designers.

Benefits available for the SoC teams:

- 1) Simultaneous and parallel debugging of hardware and software units
- 2) Accelerated debug of the peripherals (HES acts as a simulation acceleration board)
- 3) Smart Clock mechanism allowing for optimal simulation time with high speed hardware clock-driven debugging of the ARM processor code.
- 4) Verification environment based on the target devices (HES board with Actel M7 ProASIC3 FPGA).
- 5) Processor module in the hardware instead of non-100% compliant software models.
- 6) Verification of ARM7 soft core on FPGA offers logic designers and software designers a true rapid prototyping capability with the flexibility of single-chip, reprogrammable silicon.
- 7) Everybody benefits: HES hardware-accelerated simulation environment for hardware designers and high speed hardware clock-driven debugger for software developers - bridging the gap between SoC engineers.

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Applies To:

- HES (DVM 3.3) Windows
- HES (DVM 3.3) Linux
- HES (DVM 3.3) Unix