



Main Product (LNTPRO)

Installed by main installation program

Feature	Additional License Part
FRAMEWORK	
GUI, Interactive Console and Batch modes	
Macro, Tcl, Perl script support	
SUPPORTED STANDARDS	
Verilog® IEEE 1364 (1995, and 2001)	
SystemVerilog® IEEE 1800 (2005 and 2009)	
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	
RULE LIBRARIES	
ALDEC_BASIC (VHDL and Verilog) <i>Basic rules to prevent simple coding mistakes (naming, style, formatting, etc.)</i>	
ALDEC_RESTRICTIONS (VHDL and Verilog) <i>Strongly recommended rules aimed to avoid harmful chip defects.</i>	
CORE MECHANISMS	
Clocks and Resets Auto-detection <i>Design control signals are detected automatically based on direct connections to clock/reset pins and propagation through different generation schemas.</i>	
Reading and Generating SDC™ Constraints <i>ALINT-PRO can suggest constraints based on the design analysis and considers constraints specified by the user.</i>	

Feature	Additional License Part
<p>Design Constraints Extension for IP Description <i>Aldec extension for design constraints to provide the tool with information about units without RTL description.</i></p>	
<p>FPGA Vendor Library Components Support (Xilinx, Intel, Microsemi, Lattice) <i>Components from popular FPGA vendor libraries are described with block-level constraints and are properly processed by all mechanisms.</i></p>	
<p>Incremental Design Entry and Hierarchical Constraints Promotion <i>Saving performance on secondary runs by re-using previous up-to-date outputs and replacing verified blocks with properly constrained stubs.</i></p>	
<p>Finite State Machines (FSM) Extraction from RTL <i>Recognition of FSM circuits along with their properties to verify a set of dedicated rules.</i></p>	
<p>Unit and Full Mode Linting <i>Two different linting methodologies that complement each other and are usually applied at different stages of the design cycle.</i></p>	
<p>Case Analysis <i>Ability to consider isolated modes of multi-mode circuits.</i></p>	
<p>Auto-build Black Boxes for Missing HDL Design Units <i>Automatic inference of black box units based on instantiations.</i></p>	
<p>Auto-deduce Timing Properties of Black Box Pins <i>Drafts of block-level constraints based on pure topology using clock/reset properties of connected nets.</i></p>	
DEBUG CAPABILITIES	
<p>Violation Viewer <i>Displays linting results presented in form of hierarchical tree and provides various debug options (such as cross-probing, waiving, etc.)</i></p>	
<p>Waiver Editor <i>Provides means to manage violations relevance using flexible waivers mechanism.</i></p>	

Feature	Additional License Part
Configurable Reports (TXT, CSV, HTML, PDF) <i>Dumping design analysis results in different formats with a large set of filters.</i>	
TCL-based API to Linting results <i>Custom template of violations report defined via TCL script that uses a set of built-in variables.</i>	
Clocks and Reset Viewer <i>Displays list of clocks and resets along with paths of their propagation in the design and provides cross-probing options.</i>	
FSM Viewer and FSM Graph <i>Dedicated tools for state machines analysis presenting FSMs in tree-like and graphical forms.</i>	
Functional Interfaces Extraction <i>Dedicated tools for functional interfaces extraction presenting them in Elaboration Viewer.</i>	
RTL Schematic <i>Displays graphical view of a design netlist and provides large set of navigation options.</i>	SCHV required
Controls Schematic <i>Displays a schematic-like representation of the clock/reset connectivity without unrelated elements.</i>	SCHV required
DESIGN ENTRY AND MANAGEMENT	
Importing Active-HDL™, Riviera-PRO™, Vivado®, ISE®, Quartus® and Libero® Projects <i>Automatic conversion of external designs into ALINT-PRO format (including support of Xilinx Out-of-Context IPs and Coregen blocks).</i>	
File Browser <i>Provides navigation throughout design resources stored on disk.</i>	
Project Manager <i>The tool for viewing and managing projects, workspaces and their associated items.</i>	
Library Viewer <i>Displays available libraries with their contents and allows managing libraries visibility.</i>	

Elaboration Viewer

Displays the design hierarchy tree.

Feature	Additional License Part
Policy Editor <i>Provides controls to manage requirements to be verified during the design linting.</i>	
Flow Manager <i>Tool to manage design analysis process that provides quick access to the main actions and displays status of their execution.</i>	
Tasks Management <i>Ability to create custom tasks associated with the design and to trace their implementation.</i>	
SUPPORTED PLATFORMS	
Linux® (32/64-Bit)	
Windows® 10/8.1/8/7 (32/64-Bit)	

CDC Extension (LCDC)

Installed by main installation program. Additional installer should be used for ALDEC_CDC rule library.

Feature	Additional License Part
RULE LIBRARIES	
ALDEC_CDC (VHDL, Verilog, and SystemVerilog) <i>Rules for CDC and RDC verification aimed to avoid metastability issues in complex designs.</i>	
CORE MECHANISMS	
Clock Domains and Asynchronous Clock Groups Extraction <i>Detecting groups of clocks synchronous to each other, forming corresponding domains and distributing sequential elements among them.</i>	
Asynchronous Reset Domains Extraction <i>Grouping sequential elements according to their asynchronous reset signals.</i>	
Recognizing Clock and Reset Domain Crossings (CDC, RDC) <i>Detection of signals that cross clock/reset domain boundaries and require appropriate synchronization.</i>	
Multi-mode CDC Analysis (Consolidated, Case-based) <i>By default, CDC paths are consolidated throughout all possible design operation modes. Individual modes can be analyzed separately as well.</i>	
Synchronizers Patterns Recognition <i>Typical synchronization circuits used in both FPGA and ASIC designs are supported and properly considered during the CDC analysis.</i>	
Custom Synchronizers Description <i>Constraints to instruct the product which custom circuit to treat as a synchronization one.</i>	

Feature	Additional License Part
CDC Assertions Generation <i>Provides CDC assertions in SystemVerilog Assertions (SVA) format for CDC-aware simulation.</i>	
DEBUG CAPABILITIES	
CDC and RDC Reports (TXT, CSV) <i>Dump of all CDC and RDC related information, especially convenient for batch mode analysis.</i>	
CDC Viewer <i>Displays clock domains, their crossings, and synchronizers and provides cross-probing options.</i>	
RDC Viewer <i>Displays reset domains, their crossings, and synchronizers and provides cross-probing options.</i>	
CDC Schematic <i>Presents logical structure of the design suitable for analysis of CDC issues.</i>	SCHV required

Schematic Windows (SCHV)

Installed by main installation program.

Feature	Additional License Part
RTL Schematic <i>Displays graphical view of a design netlist and provides large set of navigation options.</i>	
Controls Schematic <i>Displays a schematic-like representation of the clock/reset connectivity without unrelated elements.</i>	
CDC Schematic <i>Presents logical structure of the design suitable for analysis of CDC issues.</i>	LCDC required

Optional Rule Libraries

Each rule library requires a separate installer and license part.

Rules Library	Additional License Part
ALDEC_PREMIUM (VHDL and Verilog)	LPREM
ALDEC_SV (SystemVerilog design subset)	LSV
DO-254 VHDL	LDO254-VHDL
DO-254 Verilog	LDO254-VLOG
STARC® VHDL	LSTC-VHDL
STARC® Verilog	LSTC-VLOG
RMM (VHDL and Verilog)	LRMM
RISC-V (Verilog and SystemVerilog)	LRISCV

Rule Libraries Comparison

Coverage of design areas - VHDL

	ALDEC_BASIC	ALDEC_PREMIUM	STARC_VHDL	DO254_VHDL	RMM	ALDEC_CDC
Plug-ins	ALDEC_BASIC_VHDL ALDEC_BASIC_PROJECT ALDEC_RESTRICTIONS	ALDEC_PREMIUM_VHDL ALDEC_PREMIUM_NETLIST	STARC_VHDL STARC_NETLIST STARC_PROJECT	DO254_VHDL DO254_NETLIST	RMM_VHDL RMM_NETLIST	ALDEC_CDC
naming conventions	22	4	37	2	26	7
readability, coding style	37	6	35	15	20	-
synthesis	15	9	97	49	11	-
FSM	2	17	8	7	4	-
design partitioning	-	14	4	-	2	-
simulation	3	2	9	2	-	-
clock, reset	-	11	19	11	9	29
CDC	-	1	5	-	-	16
constraints	-	-	-	-	-	6
DFT	-	-	28	-	-	-
performance, reuse	1	1	5	2	4	-
project organization	4	-	1	-	1	-
Total	84	65	252	88	77	58

Coverage of design areas - Verilog/SystemVerilog

	ALDEC_BASIC	ALDEC_PREMIUM	STARC_VLOG	DO254_VLOG	RMM	ALDEC_CDC	ALDEC_SV	RISC-V
Plug-ins	ALDEC_BASIC_VLOG ALDEC_BASIC_PROJECT ALDEC_RESTRICTIONS	ALDEC_PREMIUM_VLOG ALDEC_PREMIUM_NETLIST	STARC_VLOG STARC_NETLIST STARC_PROJECT	DO254_VLOG DO254_NETLIST	RMM_VLOG RMM_NETLIST	ALDEC_CDC	ALDEC_SV	RISC-V
naming conventions	7	4	36	2	19	7	1	0
readability, coding style	19	10	36	18	12	-	37	19
synthesis	18	7	108	57	9	-	27	46
FSM	2	19	7	7	4	-	1	10
design partitioning	-	18	4	-	3	-	-	-
simulation	10	4	18	3	-	-	-	-
clock, reset	-	11	19	11	9	29	-	3
CDC	-	1	5	-	-	16	-	-
constraints	-	-	-	-	-	6	-	-
DFT	-	-	28	-	-	-	-	-
performance, reuse	-	1	1	2	2	-	-	11
project organization	3	-	1	-	-	-	-	-
Total	59	75	263	100	58	58	66	89